## Q-Factor Definition and Evaluation for Spiral Inductors Fabricated Using Wafer Level CSP Technology

**Abstract** - A novel Q-factor definition and evaluation method are proposed for low-loss high-Q spiral inductors fabricated by using the wafer level chip size package (WLP) on silicon substrates, where the copper wiring technology with a polyimide isolation layer is used. A complex conjugate impedance matching condition is retained both at an input port and an output port of the inductor. The maximum available power gain ( $G_{AMAX}$ ) is introduced to evaluate the energy loss in one cycle. This condition provides a unique insertion loss of passive devices.







## Novel Q-factor definition and evaluation for a spiral inductor



Equivalent circuit



## Measured Q-factors derived from novel and conventional methods